

There are many paths to yield.



□

Wafers/Substrates: Thickness measurement of submonolayer native oxide films on silicon wafers

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A method has been developed for measuring the thickness of submonolayer native oxides formed on silicon wafers during rinsing. The method utilizes a rapid acid-etching process developed in our laboratory to strip the native oxide layer, followed by an analysis of the resultant solution for silicon using inductively coupled plasma optical emission spectroscopy. It was found that the method is capable of detecting and clearly determining the variations of native oxide thickness within a monolayer range with a possible  $0.2\text{\AA}$  resolution. Using this method, the growth rate of ultra-thin native oxides on a HF-cleaned silicon (100) surface was studied at room temperature during an ultrapure water rinse. Initial results indicate that the native oxide growth is significantly affected by both the exposure time of a bare silicon surface to UPW and the dissolved oxygen concentration in the water. The significance of control of the dissolved oxygen concentration in ultrapure water for advanced ULSI processes was demonstrated in a post-rinse polycrystalline silicon deposition process.

With advances in ULSI miniaturization, native oxide formation on a silicon surface and interface control are becoming critical to device performance [1-3]. Native oxides can affect quality of thin gate oxides but also provide an unfavorable increase in contact resistance for metal/Si contact formation in via holes [4-5]. Existence of native oxides on silicon surfaces also greatly affects the quality and deposition processes of polycrystalline silicon and dielectric thin films [4-6]. Selective chemical vapor deposition (CVD) and atomic layer epitaxy are especially susceptible to surface heterogeneity caused by native oxide growth [7]. Electrical characteristics of MOS field-effect transistors are also found to be adversely affected by disorder of the oxide-semiconductor interface [4-7]. In order to improve device performance and reliability, it is becoming crucial to prepare a well-defined, native oxide-free, and atomically flat surface prior to various advanced processes, including ultra-thin gate oxide growth [1-7].

Preparation of a hydrogen-terminated silicon (Si-H) surface by HF acid etching followed by an ultrapure water (UPW) rinse to remove the chemically combined fluorine is an example of the use of wet chemical pretreatment to prepare such a clean surface [8]. This pretreatment terminates the surface with a monolayer of hydrogen and passivates the chemically cleaned reactive surface to suppress native oxide growth. The questions are, how quickly does a native oxide grow on the passivated layer, and what effect does it have on subsequent processes.

The native oxide has been studied by x-ray photoelectron spectroscopy (XPS, also known as ESCA) [9-10], Auger electron spectroscopy (AES) [11], Rutherford backscattering (RBS) [12], secondary ion mass spectrometry (SIMS) [13], spectroscopic ellipsometry (SE) [14], high-resolution cross-section transmission electron microscopy (TEM) [15], and Fourier transform infrared reflection absorption

spectroscopy-attenuated total reflection (FTIR-ATR) [16]. Among these techniques, TEM, SE, and XPS were capable of measuring native oxide thicknesses of  $<30\text{\AA}$  [17]. TEM offers the only true measure of oxide thickness because it makes no assumption about atomic density, but it is not able to measure ultra-thin native oxide with a film thickness  $<10\text{\AA}$ . SE is only suitable for homogenous, smooth, reflective surfaces and oxide thickness  $>20\text{\AA}$  [18]. XPS was found to be sensitive enough to measure differences in native oxide growth on films  $<10\text{\AA}$ . Unfortunately, there has been considerable disagreement in XPS measurements from different laboratories [19]. The constants used to calculate the oxide thickness in XPS measurements were found to be sample dependent, which may be due to the moisture and organic absorbed on the silicon wafer surface.

The calibration methods used were inconsistent. In addition, the native oxide may continue growing during the wafer delivery and analysis processes. Shive and his coworkers [20] have developed a method of native oxide thickness measurement using colorimetry. They used an acid drop to extract the oxide layer to stop the growth of native oxide and then analyzed HF strippable silicon from a wafer surface colorimetrically. The molybdenum-blue method they used was found to be extremely sensitive for silicon measurement down to sub-ppm level and can also be standardized against a Si standard. However, the molybdate complexation was found to be affected by solution pH and the presence of phosphate ( $\text{PO}_4^{3-}$ ) and fluoride ( $\text{F}^-$ ) in the sample solution [20].

This paper focuses on the use of inductively coupled plasma optical emission spectrometry (ICP-OES) for characterization of ultra-thin native oxide growth. Our approach is to use the acid drop etching procedure we developed to rapidly extract the ultra-thin oxide layer and then measure the silicon concentration in the resultant solution directly without any chemical pretreatment. The initial work obtained on 200mm p-type Si (100) wafers shows that this method is able to quantitatively detect the difference in native oxide growth rate on films  $<3\text{\AA}$  (approximately a monolayer). The method can also be used for characterizing both smooth and rough silicon surfaces and both ultra-thin and thick oxide films.

## Experimental methods

**Analytical instrumentation.** All analyses were performed using a Model IRIS ICP-OES (Thermo-Jarrell Ash, Franklin, MA), equipped with a 27Hz Ar ICP source and a charge-injection device (CID) solid detector. The operating conditions for the ICP-OES include a forward RF power of 1.15kW, a reflected power of  $<5\text{W}$ , an argon coolant flow rate of 16 liters/min, auxiliary flow rate of 5 liters/min and nebulizer flow rate of 0.9 liters/min. The silicon concentration in the sample solution was determined at Si (I) 251.6 and 288.2nm lines. The amount of dissolved oxygen in the UPW used was determined colorimetrically using a R-7501 (0-1.0ppm) and a R-7512 (1-12ppm) CHEMets self-filling ampoules (CHEMetrics Inc., Calverton, VA).

**Reagents, standards, and wafers.** Hydrofluoric acid (HF) used through this work was of MB electronics grade (Ashland Chemicals, Columbus, OH). The UPW used was in-house high-purity deionized water with 18.2MW resistivity. A 10,000ppm ( $\mu\text{g/mliter}$ ) single-element standard of silicon, (NIST, Gaithersburg, MD) was used as the stock standard solution. Calibration standards were prepared by serial dilution of the stock standard and by adding the appropriate amount of HF so that the final concentration of HF matches with the sample solution (4%). The silicon wafers used in this work were polished 200mm p-type wafers with  $>5\text{Wcm}$  resistivity. The crystal orientation of the wafers was  $<100>$ . Prior to the UPW rinse, the wafers were chemically cleaned by immersing in 4% aqueous HF solution for 5 min to remove the surface thermal oxide. The oxygen-saturated UPW used in this work, unless otherwise noted, contains approximately 6ppm dissolved oxygen.

**Sample preparation.** Experiments were designed and performed to assess the ultra-thin native oxide growth on a HF-treated silicon surface during a very short UPW rinse. In practice, the samples were prepared in the following manner: Before each experiment, a wafer was always cleaned by immersion

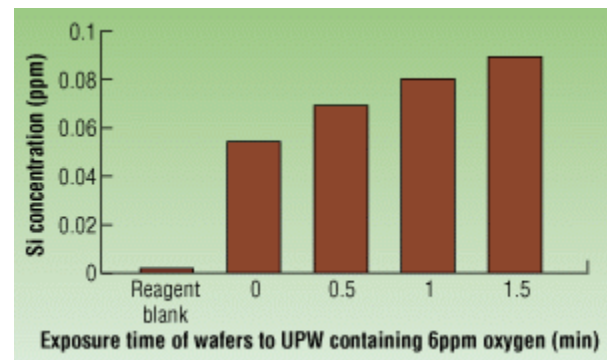
in 4% aqueous HF solution for 10 min. The wafer was taken out of the 4% HF bath, immersed in a UPW bath for a couple of seconds to remove residue HF on the surface, then quickly transferred to another UPW bath for rinsing experiments at various times. With a 4% HF, the oxide layer formed during the UPW rinse was stripped off the wafer, being converted into an aqueous solution. The resultant solution was then directly introduced, via a conventional nebulizer without any chemical pre-treatment, into the ICP for silicon determination.

## Results and discussion

**Effect of UPW rinse time.** The thermal oxidation of the silicon surface at elevated temperatures in either dry oxygen ( $>200\text{\AA}$ ) or steam can be characterized by the Deal and Grove relationship [21]. However, the formation of native oxide on a silicon surface at room temperature has not been well understood. Ohmi [1-2] has studied the growth of native oxide during a UPW rinse within a relatively long period of time (e.g., 1 hr and 60 days) using XPS. His work indicated that native oxide was formed on a silicon surface during a UPW rinse process due to the presence of dissolved oxygen. He also found that the thickness of native oxide on a n-type Si (100) surface increased with increasing the concentration of dissolved oxygen and the exposure time of a wafer surface to UPW. The surface roughness was also gradually increased [1-2].

*Figure 1. The effect of UPW rinsing time on the native oxide growth at room temperature.*

Our work was intended to focus on the effect of a short UPW rinse (e.g.,  $\leq 10$  min) on the growth rate of native oxide so that the initial stage of the native oxide formation could be studied. A plot of the silicon concentration found in the 4% HF stripping solution vs. oxygen-saturated UPW rinse time, ranging from 0 to 10 min, is given in Fig. 1. The silicon concentration was typically measured by ICP-OES at Si (I) 251.6nm line. The silicon wafers used in this study were 200mm p-type with  $>5\text{Wcm}$  resistivity. The crystal orientation of the wafers was  $\langle 100 \rangle$ . The amount of dissolved oxygen in the UPW used was 6ppm.



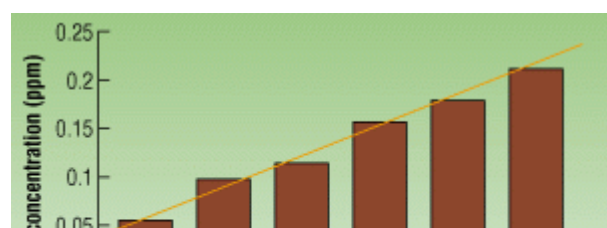
The amount of silicon found in the HF stripping solution increases almost linearly with increasing exposure time of wafers to oxygen-saturated UPW (Fig. 1). This rate behavior is different from the parabolic relationship obtained by Ohmi and his coworkers [1-2, 22] in their relatively long time rinsing studies, suggesting that the oxidation mechanism may be different during the short time frame of a UPW rinse typical for wafer cleaning today.

Figure 2 shows the behavior of silicon concentration obtained by ICP-OES as a function of an even shorter UPW rinse time (within 1.5 min). Similar rate behavior was observed when the silicon concentration was increased as the exposure time of the wafer to oxygen-saturated UPW is increased. The reagent blank was found to be low compared to the silicon concentrations in the etching solution and did not show evidence of any interference. The silicon concentration obtained at 0-min rinse time was unexpectedly high, however, as observed in Fig. 1.

*Figure 2. Early time study showing the effect of UPW rinse on the native oxide growth.*

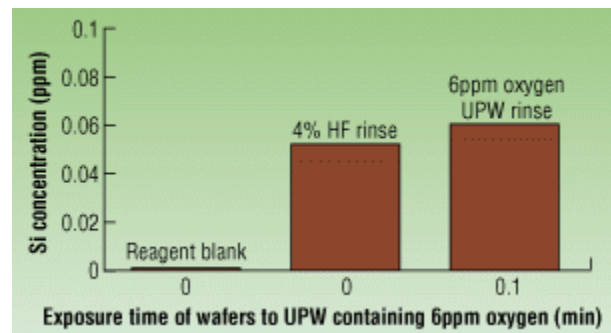
### Root cause of high silicon signal at zero minutes.

Although it can be subtracted as a method blank, the substantial Si signal observed at 0-min rinse would



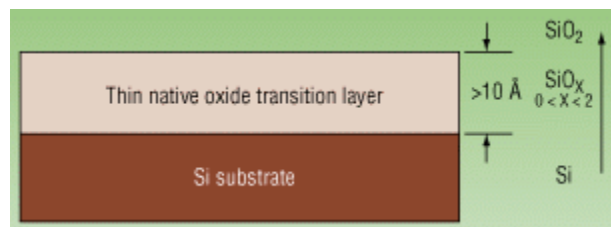
somewhat restrict the detection limit of silicon for native oxide thickness measurement and may also lead to an overestimation of native oxide thickness. The ICP-OES spectral interference was first investigated by simultaneously monitoring the Si (I) 212.4nm, 251.6nm, and 288.1nm lines. The same results obtained suggest that the high silicon results were not caused by spectral interference. The reagent blank obtained, as shown in Fig. 5, was extremely low, indicating that there was no noticeable silicon contamination from the reagents, the centrifuge tubes, the container used for HF stripping, and laboratory environment. A true zero minute UPW rinse was studied because we suspected that some native oxide may be quickly formed during the initial 2-sec UPW rinse for the purpose of removing residue HF and any dissolved silicon on the surface after the HF dip (see sample preparation in experimental methods section). A wafer taken out of the HF bath was immersed in another clean 4% HF bath for 5 sec then quickly stripped and analyzed. Figure 3 shows a comparison of the result obtained with 5 sec-UPW rinse. It can be seen that the silicon concentration obtained with 5-sec HF rinse (true zero minute UPW rinse) is still substantially high and comparable with that obtained with 5-sec UPW rinse, indicating that the amount of native oxide formed during this rinse is minimal. The high silicon result was likely due to the dissolution of the silicon substrate when HF was used to strip the oxide layer for sample collection.

Figure 3. Investigation of the root cause of high Si blank.



What causes this dissolution of silicon substrate? A slow oxidation of hydrogen-terminated and passive surface is followed by a fast removal of surface oxide by HF during the stripping. The oxidation-dissolution processes could occur during and after the ultra-thin native oxide is removed. Higashi and coworkers [24] used dilute HF solution to prepare a hydrogen-terminated silicon surface and found that the diluted HF solution induced microscopic roughness on both Si (111) and Si (100) surfaces, while concentrated HF solutions do not alter the surface morphology. Their results suggested that the microscopic surface roughness was due to dissolution of the silicon surface in diluted HF solution. Since HF acid itself does not etch the silicon surface, the H<sub>2</sub>O and/or dissolved oxygen in diluted HF solution would have to be responsible for the oxidation [23]. This is further supported by the silicon dissolution studies done by Ogawa and coworkers [24] on both Si (100) and Si (111) surfaces using FT-IR-ATR. Their results seem to indicate that the dissolved oxygen in HF solution is responsible for the oxidation of the silicon surface.

Figure 4. Computer-generated cross-sectional schematic diagram of Si-SiO<sub>2</sub> interface.



Given that the silicon substrate is continuously dissolved in the diluted HF solution used to strip the oxide layer, this phenomenon subsequently leads to an overestimated silicon reading for the native oxide measurements. Since the concentration of HF stripping solution used and the stripping time are fixed, the amount of stripped silicon from the silicon substrate is expected to be constant. Therefore, the silicon concentration observed at 0-min UPW rinse was subtracted as a method blank from all other obtained results. It should be noted, however, that some other factor besides silicon dissolution might be the cause of the high silicon concentration observed at 0-min rinse.

**Conversion of silicon concentration to oxide**

Native oxide thickness as a function of oxygenated UPW rinsing time (min)

**thickness.** The conversion of stripped Si concentration to oxide thickness was found to be difficult due to lack of enough information on the structure and density of the ultra-thin native oxide formed. The literature [25-27] has indicated that ultra-thin native oxide (10-100Å) formed on the silicon surface is essentially a heterogeneous mixture of "SiO" and "SiO<sub>2</sub>". At the interface of this Si-SiO<sub>2</sub> structure, oxides thinner than 20Å are not fully stoichiometric, and there is a transition region in Si-SiO<sub>2</sub> structure (Fig. 4). The XPS studies of the 2p electron spectral line of silicon atoms showed that the oxide has the form SiO<sub>x</sub>, with x increasing from 0 to 2 as the distance from the silicon surface increases to greater than at least 10Å [27]. One way of estimating the thickness of the native oxide is to use surface concentrations (atoms/cm<sup>2</sup>) by assuming that a monolayer (~4Å) of oxide has approximately 2.0x10<sup>15</sup> atoms/cm<sup>2</sup>.

Figure 5. Surface concentrations of Si, SiO, and SiO<sub>2</sub> vs. UPW rinsing time.

The surface concentration of silicon in atoms/cm<sup>2</sup> was calculated based on solution concentrations of stripped silicon, volume of the stripping solution, atomic mass of silicon, Avogadro constant (6.023x10<sup>23</sup>), and surface area of the wafers (314cm<sup>2</sup> for 200mm wafers). However, the surface concentrations of SiO and SiO<sub>2</sub> were calculated based on the theoretical mole ratios.

Suppose the form of native oxide on the silicon surface is SiO and one mole of silicon is bonded with one mole of oxygen. The total number of the atoms (Si + O) in monoxide form should be twice the number of oxidized surface silicon atoms. For example, if the calculated silicon surface concentration is 2.0x10<sup>14</sup> atoms/cm<sup>2</sup>, the SiO surface concentration will be 4.0x10<sup>14</sup> atoms/cm<sup>2</sup>. If the form of the native oxide is completely SiO<sub>2</sub> and one mole of silicon is bonded with two moles of oxygen (mole ratio 1:2), the SiO<sub>2</sub> surface concentration will be 6.0x10<sup>14</sup> atoms/cm<sup>2</sup>.

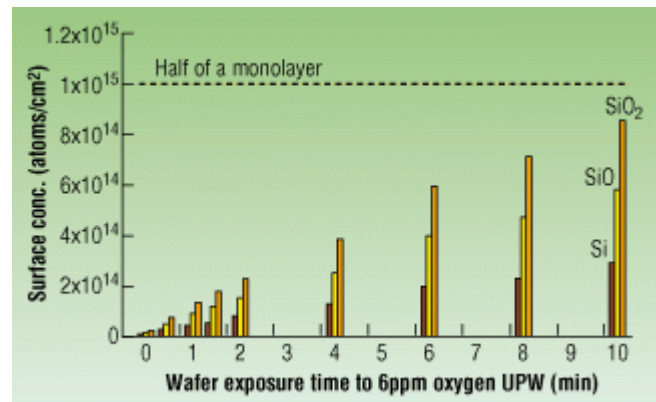


Figure 5 shows the surface concentrations of extractable silicon as well as surface concentrations of SiO and SiO<sub>2</sub> as a function of wafer exposure time to oxygen-saturated UPW. Although the composition of native oxide is unknown, it is clearly evident that the analytical method described in this work is able to monitor and determine the variations of ultra-thin native oxide growth. These can be caused by varying process conditions. Since SiO<sub>2</sub> is the extreme, the results elucidated in Fig. 4 suggest that the thickness of the native oxide formed on a p-type Si (100) surface resulting from a <=10 min of oxygenated UPW rinse was less than half of a monolayer. By assuming, for the purpose of calculation, the native oxide to be fused or amorphous quartz with a density of 2.2 gm/cm<sup>3</sup> as other researchers have used [20], the silicon concentration can also be converted to oxide (SiO<sub>2</sub>) film thickness in angstroms (see table). The film thicknesses calculated in angstroms match those corresponding to the surface concentrations calculated in atoms/cm<sup>2</sup>. For example, the SiO<sub>2</sub> surface

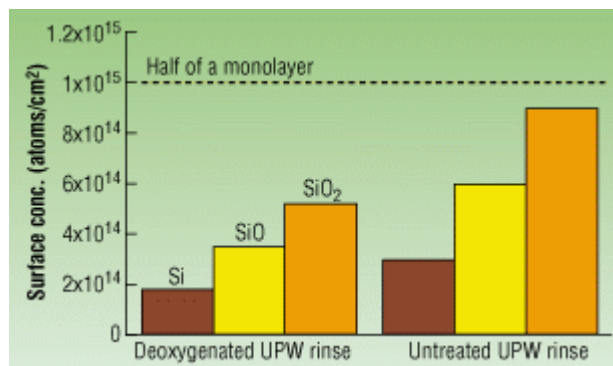
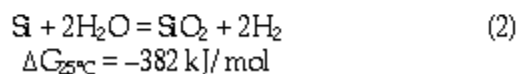
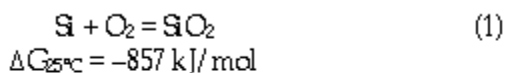
concentration calculated from the 10-min oxygenated UPW rinse indicated approximately half of a monolayer ( $<1.5\text{\AA}$ ) oxide formed on the silicon surface, while the calculated thickness based on the fused quartz ( $\text{SiO}_2$ ) was  $1.32\text{\AA}$ . It should be kept in mind that the density of the native oxide with a thickness less than a monolayer may not be  $2.2\text{ gm/cm}^3$ . Furthermore at the interface, the ultra-thin native oxide may have large quantities of  $=\text{Si}=\text{H}_3$  and  $\equiv\text{Si}-\text{H}$  bonds [23] and may have an average form of  $\text{SiO}_x$  with  $x$  between 0 and 1, that is,  $\text{Si}_2\text{O}$ , without considering the hydration. This is further supported with the results described by Deal and Kao using a pulsed laser atomic probe [3].

TABLE A case study. In a fab, engineers in two different locations were depositing polycrystalline silicon on a bare silicon surface. Prior to the deposition, the wafers were treated with dilute HF, rinsed with UPW, and dried. The equipment used to clean the wafers and to deposit the poly-Si was exactly the same in both locations. However, the end result of the poly-Si deposition was quite different, with one location producing useless product. The sizes of the grain grown at that site were found to be unfavorably large and not uniform. The grain distribution was also uneven. Surface contamination was suspected and a study was undertaken to identify any unwanted metallic or organic surface contamination. However, XPS, SIMS, and GC-MS found no contaminants. Knowing that poly-Si will not deposit satisfactorily if an oxide is present on the surface, we made a measurement of the amount of native oxide on the wafer surface using the method described here. It was found that the wafers cleaned for 10 min at the two sites contained different amounts of oxide on the surface (Fig. 6).

Further studies were then conducted to determine the exact nature of the difference between the two sites and how that difference affected the wafer, the amount of oxide on it, and the relationship between the oxide thickness and poly-Si deposition problem. It was found that the UPW systems used at the two sites were slightly different. The dissolved oxygen measurements showed that one UPW system contained 50ppb  $\text{O}_2$  while the other contained 6ppm. It was the latter system that produced more oxide on the silicon surface and caused the poly-Si deposition failures. Due to the existence of more native oxide on the silicon surface, which formed a heterogeneous and rough silicon surface, it was difficult to grow high-quality and uniform polycrystalline silicon. This study showed that it is important to control oxide growth even in the submonolayer concentrations, to produce quality poly-Si. This may also be true for other semiconductor processes [1-2].

Figure 6. Effect of oxygen-containing and deoxygenated UPW rinse on the native oxide growth.

An important question naturally arises. Is dissolved  $\text{O}_2$  in UPW solely responsible for the native oxide formation on silicon surface during a UPW rinse? Based on the thermodynamics theory,  $\text{O}_2$  and  $\text{H}_2\text{O}$  can both oxidize silicon to form  $\text{SiO}_2$ . The oxidation reactions may be represented by the following equations [28]:



The calculations of Gibbs free energy at room temperature ( $\Delta G_{25^\circ\text{C}}$ ) showed that the reactions in

Eqns. 1 and 2 are both spontaneous, with the reaction in Eqn. 1 having a greater tendency toward the formation of  $\text{SiO}_2$  [29]. Interestingly, Ohmi's kinetics work [27] showed that the native oxide hardly grew on silicon surfaces at room temperature during a seven-day exposure of wafers to dry air. He indicated that native oxide growth on the silicon wafer surface at room temperature required coexistence of  $\text{O}_2$  and  $\text{H}_2\text{O}$  [22, 30-32]. It is possible that Si-H bonds on the hydrogen-terminated surface are easily converted into Si-O-Si or Si-OH in the presence of  $\text{H}_2\text{O}$  [22]. Another possibility would be that the dissolved  $\text{O}_2$  or  $\text{OH}^-$  attacks the interior Si-Si bonds without breaking the Si-H bonds. Although the growing mechanism of native oxide has not been understood, it seems that the native oxide formation is largely determined by reaction kinetics rather than thermodynamics alone.

## Conclusion

ICP-OES has proved to be a suitable and sensitive analytical technique for the characterization of ultra-thin native oxide formed on silicon surface. By coupling with the rapid acid-etching method developed in our laboratory, ICP-OES is capable of detecting and clearly determining the variations of native oxide growth within a monolayer range with a possible  $0.2\text{\AA}$  resolution. Since the native oxide layer can be chemically stripped and converted into an aqueous solution within 30 sec, it is possible to obtain real-time surface information with an off-line measurement. The formation of native oxide on silicon surface resulting from various wet surface processes could then be representatively evaluated without experiencing the continuous oxidation problem. The method is simple, reproducible, and standardizable to NIST standards. The analysis is also found to be free of both spectral and matrix interference.

Evidence is presented in this work that the silicon signals due to the dissolution of silicon substrate at the HF stripping step become crucial since the overall silicon concentrations being detected by ICP-OES are very low. To suppress the dissolution of silicon substrate and improve the signal-to-background ratio, the stripping time may need to be shortened and the dissolved oxygen concentration in HF solution reduced. The conversion of silicon solution concentrations obtained by ICP-OES to oxide thickness is greatly dependent on the understanding of the structure and growing mechanism of the ultra-thin native oxide on silicon surface. Since it is the most stable form,  $\text{SiO}_2$  with a density of  $2.2\text{ gm/cm}^3$  was used as the form of the native oxide to calculate oxide thickness ( $\text{\AA}$ ) in order for different laboratories to make a direct comparison.

Initial results show that ultra-thin native oxide is grown immediately at room temperature on a HF pre-cleaned p-type Si (100) surface during an oxygenated UPW rinse. The initial growth rate is found to increase linearly with increasing exposure time of the silicon surface to UPW during the first 10 min of oxygen-saturated UPW rinse. The results obtained with deoxygenated UPW (containing  $\sim 50\text{ppb}$  dissolved oxygen) rinse indicate that the native oxide formation on the silicon surface can be reduced by decreasing the dissolved oxygen concentration in UPW.

Future investigations of native oxide formation, kinetics, and control will include obtaining a better understanding of the effects of oxygen content in deionized rinse water on growth mechanisms and other properties of these films. Also, studies will be carried out in controlled environments (gas or vacuum) to determine mechanisms involved in native oxide formation, as well as to minimize adverse effects on device performance. In this case, integrated processing (cluster system) techniques will be employed. Such studies may also lead to similar investigations involving chemical oxides.

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## References

1. T. Ohmi, Proc. 10th SPWCC Conference, M.K. Balazs, ed., Balazs Analytical Laboratory, Sunnyvale, CA, p. 251, 1991.
2. T. Isagawa, M. Kogure, T. Imaoka, T. Ohmi, Proc. 11th SPWCC Conference, M.K. Balazs, ed., Balazs Analytical Laboratory, Sunnyvale, CA, p. 224, 1992.
3. B.E. Deal, D.B. Kao, Proc. Tungsten and Other Refractory Metals for VLSI Applications, E.K. Broadbent, ed., Materials Research Society, p. 27, 1987.
4. B. E. Deal, C. R. Helms, "Vapor Phase Wafer Cleaning Technology," Handbook of Semiconductor Wafer Cleaning Technology, W. Kern, ed., Noyes Publications, NJ, p. 274, 1993.
5. M. Miyawaki, Y. Shilbata, T. Ohmi, IEEE Electron Device Letters, 11, 448, 1990.
6. N. Hirashita, M. Kinoshita, I. Aikawa, T. Ajioka, Proc. 6th Int'l Symp. on Silicon Materials Science and Technology, H.R. Huff, K.G. Barrachough, J. Chilawa, eds., The Electrochemical Society, Pennington, NJ, p. 313, 1990.
7. S. Takami, Y. Egashira, H. Komiyama, Jpn. J. Appl. Phys. 36, 2288, 1997.
8. G.S. Higashi, Y.Chabal, "Silicon Surface Chemical Composition and Morphology," Handbook of Semiconductor Wafer Cleaning Technology, W. Kern, ed., Noyes Publications, NJ, p. 455, 1993.
9. J.E. Fulghum, Surface and Interface Analysis, 20, 161, 1993.
10. F. Yano, A. Hiraoka, T. Itoga, H. Kojima, K. Kanehori, Y. Mitsui, J. Vacuum Science & Technol., 13, 2671, 1995.
11. C.C. Chang, D.M. Boulin, Surface Science, 69, 385, 1997.
12. O.L. Krivanek, D.C. Tsui, T.T. Sheng, A. Kamgar, The Physics of SiO<sub>2</sub> and Its Interfaces, S.T. Pantelides, ed., Pergamon, New York, 1978.
13. H. Yamazaki, M.Takahashi, Surface and Interface Analysis, 25, 937, 1997.
14. G.E. Jellison, J. Appl. Phys. 69, 7627, 1991.
15. M.J. Kim R.W. Carpenter, J. Mater. Res., 5, 347, 1990.
16. M. Hirose, et al., Solid State Technology, 43, 1991.
17. J.R. Shallenberger, et al., Oxide Thickness Determination by XPS, AES, SIMS, RBS, and TE, Charles Evans & Associates, Redwood City, CA, 1998.
18. H. Reisinger, H. Oppolzer, W. Honlein, Solid State Electronics, 35, 797, 1992.
19. S. Iwaata, A. Ishizaka, J. Appl. Phys., 79, 6653, 1996.
20. K. Vepa, K. Buker, L.W. Shive, Proc. Cleaning Technology in Semiconductor Device Manufacturing IV, R.E. Novak J. Ruzyllo, eds., The Electrochemical Society, Pennington, NJ, p. 358, 1995.
21. B.E. Deal, A.S. Grove, J. Appl. Phys., 36, 3770, 1965.
22. M. Morita, "Native Oxide Films and Chemical Oxide Films," Ultraclean Surface Processing of Silicon Wafers, T. Hattori, ed., Springer, NY, p. 543, 1998.
23. G.S. Higashi, Y.J. Chabal, G.W. Trucks, K. Raghavachari, Appl. Phys. Lett., 56, 656, 1990.
24. H. Ogawa, K. Ishikawa, M.T. Suzuki, Y. Hayami, S. Fujimura, Jpn. J. Appl. Phys., 34, 732, 1994.
25. R.A. Clarke, et al., J. Electrochem. Soc., 122, 1347, 1975.
26. Y.J. Chabal, G.S. Higashi, K. Raghavachari, V.A. Burrow, J. Vac. Sci. Technol., 7, 2104, 1989.
27. M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, K. Suma, Appl. Phys. Lett., 55, 562, 1989.
28. S. Takami, Y. Egashira, H. Komiyama, Jpn. J. Appl. Phys., 36, 2288, 1997.
29. S.P. Parker, ed., Physical Chemistry Source Book, McGraw-Hill Book Co., NY, 1988.
30. M. Morita, et al., Jpn. J. Appl. Phys., 29, L2392, 1990.
31. T. Ohmi, Proc. 15th SPWCC Conference, M.K. Balazs, ed., Balazs Analytical Laboratory, Sunnyvale, CA, p. 157, 1996.
32. T. Ohmi, et al., J. Electrochem. Soc., 137, 1008, 1990.



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