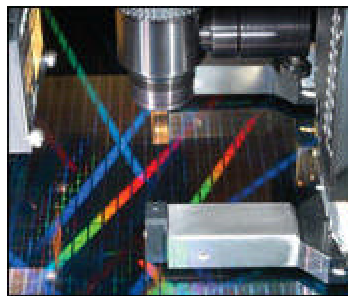
There are many paths to yield.

Meeting 2001 ITRS Challenges

Overview



The elastic metal probe arm of the Solid State Measurements FastGate metrology system performs C-V measurements in a wafer scribe line. (Photo courtesy of Michael Ray)

While the 2001 ITRS is a roadmap for sustaining IC technology, underlying manufacturing capabilities will be based on solutions from this industry's equipment, materials, and software suppliers. Negotiating potholes, detours, and even "red-flagged" roadblocks on the 2001 ITRS, executives from a broad range of industry suppliers highlight new solutions and breakthroughs that may make the road passable.

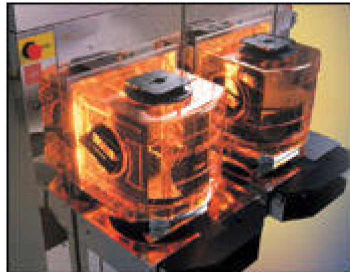
The worldwide mix of semiconductor industry technologists who produced the 2001 International Technology Roadmap for Semiconductors (ITRS) clearly defined "useful guidance for suppliers of equipment, materials, and software and clear targets for researchers in outer years." The ICs cited in the ITRS will come from the likes of Intel, TI, TSMC, NEC, and many others, but innovative abilities to manufacture these chips will come from Applied Materials, TEL, Novellus, Canon, Lam, and many others on the long list of industry suppliers.

Knowing that most solutions to ITRS challenges will come from these companies, Solid State Technology polled senior executives to brief us about significant solutions that address roadmap problems and associated caveats.

Metrology, defects

The 2001 ITRS dubs metrology the "essential enabler," linking it to fundamentals such as yield improvement, ramping success, the cost of manufacturing, chip diversity, and time to market.

Important near-term ITRS challenges for metrology involve materials and processes for gate stacks (see "Metrology's link to materials," p. 43), ultrashallow junctions, and copper low-*k* interconnects. There is a growing call for full 3-D measurement for sub-90nm contacts and vias, transistor gates, interconnect lines, and active area measurements instead of test structures. Some metrology must be capable of atomic distance measurements (see "ITRS wants to see a small world," p. 44). On the defect side of metrology, detecting those associated with high-aspect-ratio structures is particularly crucial.



Wafer carriers from Rudolph Technologies.

Not specifically part of metrology challenges, many specifications, particularly ITRS materials and defect requirements, imply a need for increasingly robust surface and chemical analytical capabilities (see "Cutting-edge analytical laboratory capability," p. 46).

Gates, stacks

"Needs with the five-year direction toward 8Å equivalent oxide thicknesses (EOTs), complex materials stacks, and interfacial properties portend a trend back to first principles and electrical measurements of properties," says William Alexander, VP at Solid State Measurements (SSM), Pittsburgh, PA. "We must measure precisely and directly what we intend to control. Contacting C-V measurement is the 'gold standard' for thin-film metrology," says Alexander, "but has infrequently been used in fabs because contacts are destructive and the method creates delays."

SSM has developed a nondamaging, noncontaminating Elastic Metal gate (EM-gate) probe that instantaneously provides temporary contact for C-V and I-V metrology for true electrical characterization of dielectrics and interfaces, within conventional scribe lines, in real time on product wafers at production speeds. "At several IDM labs, first-generation tools are routinely measuring EOTs down to 7Å with 0.01nm precision. And we are working to prove precision of 0.0035nm or better," says Alexander.

"In addition to thickness, ITRS challenges call for determination and control of multilayer stack interfacial properties, and oxynitride and high-*k* dielectric composition," says Jean-Claude Fouéré, GM at SOPRA Inc., Westford, MA. SOPRA, in collaboration with several R&D labs and International Sematech, has developed spectroscopic ellipsometry (SE) capability that extends the spectral range to 145nm wavelength (VUV) and combines it with grazing incidence x-ray reflectometry (GI-XRR). This method's value is in characterizing individual layers of, for example, an SiO_2-$SiON_x$-SiO_2 high-*k* dielectric stack (Table 1).

Table 1. VUV-SE and GI-XRR look at a gate stack (3s)

Structure	Thickness (nm)	SiN_x composition (%)
Surface roughness	0.16 ± 0.05	NA*
SiO_2	0.58 ± 0.5	NA
SiO_xN_y	2.01 ± 0.2	24 ± 4
SiO_2	1.03 ± 0.05	NA

*NA = not available

Source: SOPRA

Fouéré explains, "Each measurement is done at the same location and time, and regression analysis is performed on two complementary sets of measurements. Each technique alone cannot achieve the same results because of the relatively small difference in index of refraction between materials and low atomic numbers."

Cross-sectional metrology

ITRS requirements for 3-D metrology (e.g., characterizing resist profiles or shallow trench isolation structures, including film thicknesses and wall angles) can be met with FEI's integration of a focused ion beam (FIB) and scanning electron microscope (SEM). Steven Berger, CTO at FEI, Hillsboro, OR, says, "This technology provides cross-section metrology on product wafers that can be returned to production (Fig. 1). There is also a throughput or time-to-data advantage."

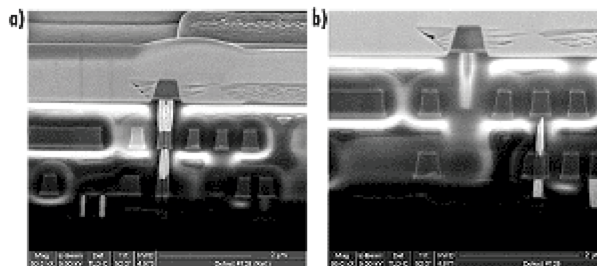


Figure 1. An electrical fault detected by an inspection system subsequently exposed to show incomplete etch and missing metal lines when compared to reference data (left). (Source: FEI)

One application of combined FIB-SEM technology finds killer defects in copper. Berger says, "The emerging technique of choice for detecting killer defects in copper is voltage contrast inspection. A killer defect discovered by this approach is often subsurface and can only be analyzed by structural metrology."

Atomic force microscopy

Not all ITRS metrology needs require improving the underlying technology. Atomic force microscopy (AFM), for example, has the capability to meet surface roughness, in-die dishing, and erosion and flatness measurements, particularly for CMP. Bradley Todd, director of marketing at Veeco Instruments, Santa Barbara, CA, says, "Only AFM achieves negligible lateral force that leaves devices undamaged and has the necessary spatial resolution due to linearity and precision of its three closed control loop axes."

However, the roadmap does challenge "the throughput and fab friendliness of AFM." Todd says, "We are working on higher throughput for next-generation systems that are more fab friendly and supplying

resources necessary to stay current with 300mm automation so that all systems fit quickly and seamlessly into automated fabs."

A bit of development work that may help AFM is found in efforts to produce faster, more accurate, and higher-resolution scanning for nanopositioning. Max G. Lagally, chairman at Piezomax Technologies, Madison, WN, says, "We have found that scanners that operate with closed-loop feedback using capacitive sensing techniques can achieve precision required by AFMs."

Briefly described, flexure-guiding mechanisms are used to achieve a pure, independent, single-axis (x-, y- or z-) motion with minimal parasitic errors. These mechanisms constrain off-axis motion and combine piezo-actuators and sensors to form an integral stage subsystem. Stages have wide dynamic range and quick response (less than a few msec/&mum-step) and provide ultrasmooth positioning and true planar motion. Noncontact capacitance sensors provide positioning measurement and feedback control with high stability, resolution, and wide bandwidth.

Lagally says, "Positioning noise can be as low as 0.5nm for scanners with large motion directions (= 100&mum) and 0.1nm for scanners with short motions (= 20&mum), leading to designs that exceed conventional positioning methods. In addition to AFMs, aspects of this technology are applicable to steppers where present overlay control is 45nm, 3s."

HARI defects

The ITRS specifically names high-aspect-ratio inspection (HARI, detection into structures with an aspect ratio >3) as a difficult challenge. The technical problems are poor transmission of energy into and back out of such structures and the large number of them per wafer. One revolutionary technology that addresses HARI is patented direct digital holography (DDH) from nLine Corp., Austin, TX, which is capable of inspecting aspect ratios = 12:1.

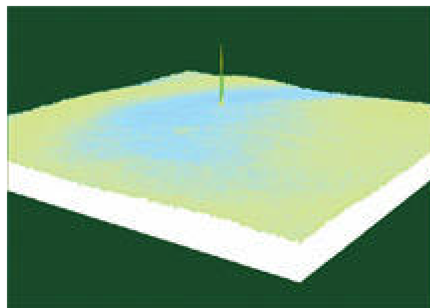


Figure 2. 3-D phase image of a single defective contact — 50nm of residual oxide in the bottom of a 220nm contact, 1500nm deep — detected in an array of millions of good contacts. (Source: nLine)

DDH creates a hologram by combining reference and object beams of reflected coherent light. This combination creates a complex pattern of interference fringes that contains information about the intensity and phase of the reflected light. The DDH technique captures the hologram with a CCD, then separates it into intensity and phase images. The latter represents the phase of the light falling at every pixel, which is a function of path length between the inspected surface and the camera. The phase image can be converted to a topographic map of the inspected surface with remarkably high vertical resolution (Fig. 2). Potential defect detection sensitivity for DDH is ~1/13th the illumination wavelength (e.g., ~20nm for 266nm illumination) and is limited only by optical noise within the

system.

Bob Owen, nLine CEO, says, "The aspect ratio of the minimum detectable volume doesn't matter in DDH for small defects; the defect can be short and broad, tall and thin, cubic, whatever. Equal volumes give equal signals independent of their aspect ratios."

Factory integration, yield

Treated in separate chapters, 2001 ITRS factory integration and manufacturing yield requirements can be summarized as managing complexity. "Rapid changes in semiconductor technologies, business requirements, and market conditions are making effective and timely factory integration to meet accelerated ramps and yield targets more difficult over time." Adding to the complexity, "today, globally disparate semiconductor factories have to run as a single 'virtual factory' while meeting geographical regulations and managing complex supply chains."

Roadmap integration specifications emphasize critical requirements for software solutions (e.g., complex embedded controller software to enable connections between equipment), standard interfaces, and factory forecasting and flexibility. Other specifications call for agile manufacturing, 100% automated material handling system (AMHS) interbay and intrabay systems (see "Unified AMHS," p. 48), advanced process control, scheduling and dispatching, and e-diagnostics.

"New software technologies take advantage of faster, integrated metrology, and are directly linked to higher yields," says Russell Ellwanger, GM of Applied Materials' Process, Diagnostics, and Control Business Group, Santa Clara, CA. Applied's Defect Source Identifier (DSI) package, for example, lets engineers instantly process data from in-line defect review systems and rapidly match defect information with a large library of known defect types. It then presents a weighted probability of defect sources based on a global history of operations for given processes, and suggests corrective tool actions.

"Other advances include sophisticated tool health monitoring and diagnostics that let fabs go beyond pre-determined system maintenance schedules to run tools as long as process performance remains in specification. This can significantly elevate uptime and availability, and cut maintenance costs," Ellwanger says.

The industry's faster introduction of process technology advances and ramps to production target yields requires a systematic, engineered approach to yield management. Fault isolation complexity is expected to grow exponentially, combining the difficult tasks of defining fault dimensions horizontally and vertically. It is especially difficult to analyze circuit failures that leave no detectable physical remnant. Accordingly, new analysis tools and techniques that can isolate nonvisual failures are needed. Part of this involves optimizing IC designs for a given process capability and testability within the realm of optimum yields.

"A challenge at the 65nm node is yield dependence on layout-circuit interactions with manufacturing processes and soft failures," says John Kibarian, CEO, PDF Solutions, San Jose, CA. An example is highly resistive contacts that only occur under certain processing or layout conditions and are difficult to detect and diagnose because they can manifest themselves as a circuit-timing problem or a test vector that seems to fail frequently.

"Traditional yield models are no longer sufficient, as they are typically modeled as a function of defect density, and chip area systematic yield loss typically comprised <5%," says Kibarian.

PDF Solutions continues to develop tools and methodologies to introduce a more comprehensive set of design attributes to model yield. These attributes are related to the physical understanding of layout-dependent failure modes. PDF's technologies enable extraction of relevant attributes from product layouts and can include parameters such as the number of contacts or vias as a function of

neighborhood layout density or the underlying topography of copper interconnects.

Traditional techniques must also be enhanced by new electrical test methods to minimize yield losses, including those from soft failures. PDF Solutions accomplishes this with improved defect localization techniques from product test data and by designing special test chips — characterization vehicles (CVs) — that can be made sensitive to specific failure modes. CVs can be designed to span the product layout space to uncover random and systematic defects that result in both hard and soft failures. "By mimicking product layout attributes, CVs can uncover layout-process interactions. Specific models can also be developed for each chip functional block," says Kibarian.

Communications
"Most semiconductor manufacturers agree that equipment and process information must be shared both fabwide and worldwide for effective semiconductor-manufacturing management," says Joseph G. LaChapelle, GM of the EGsoft Division of Electroglas Inc., San Jose, CA. "But there has been a fundamental disconnect between equipment and processes, the plant floor and external systems, and the fab enterprise with its partners." ITRS says factory integration must work in "a synchronized way to profitably produce complex products for a time-sensitive market."

The Electroglas approach to a solution — collaborative process management (CPM) — connects processes through a secure web-based software framework that collects, stores, and presents an enterprise-wide data set for analysis, statistically valid data mining, experience-based results correlation, and corrective action. It incorporates flexible software operating rules that adapt to a specific factory. The software framework is constructed to be reusable with a common software toolset that allows rapid development and deployment of customized analysis tools in a global environment.

Applied's Ellwanger says, "Many industry suppliers are working on data mining, using automated analysis algorithms to sift through complex parametric, process inspection, and equipment information; pinpoint problem areas; and then identify possible actions. Data mining can identify key factory data metrics, such as yield, tool uptime, and utilization." For example, at the tool level, data mining might identify a specific defect type as a primary yield detractor, then determine that it results from a particular system's low exhaust pressure during etching.

Electroglas' CPM is also equipped to correlate test results with optical defects through CAD navigation and failure analysis software that performs defectivity analysis and overlays the result with design layout from a CAD navigation database. It identifies electrical test or parametric failures with design and uses failure analysis data on nonvisual killer defects to locate them in the design. CPM provides feedback to design as well, to manage or adjust it to match the process capability of a manufacturing line. While specific details are proprietary, LaChapelle notes that "backend customers using CPM have reported a 3-6% increase in yield, and as much as 20% in throughput."

Accessing tool information via a SECS/GEM-compliant station controller has been a bottleneck, says Charles Baylis, CTO, domainLogix. The new object-oriented equipment model standard being developed under Semi should allow direct access to tools by client software applications, says Baylis.

Robotic interfaces
Part of the ITRS factory automation challenge involves bringing science to mechanical robotic alignment to maximize tool uptime and utilization. Addressing this challenge, engineers at MicroTool, Colorado Springs, CO, have developed systems for measuring adjustments and determining robot teach points, all designed to assure precision and consistency among mechanical interfaces across a fab.

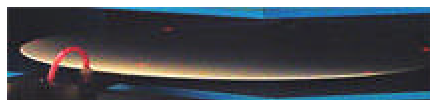


Figure 3. MicroTool target wafer on a robot end effector, showing sensor head and light beam spots.

MicroTool's VP of fab solutions, Charlie Huff, says, "These tools give equipment engineers a means of maintaining mechanical interoperability." The MicroTool system replaces traditional eyeball-alignment practices with a calibrated system of precision sensors (Fig. 3). By aligning an entire equipment set with a single method, equipment engineers can substantially reduce the effects of automation complexity by applying mechanical alignment as an integrating force across the fab, cutting downtime and unscheduled maintenance.

Huff says, "One user reports that a MicroTool system reduced setup time on a wafer sorter by four hours. Another engineer told us that an all-day process to align a robot was reduced to ~30 min."

Advance process control

The 2001 ITRS is very clear on the looming importance of advanced process control (APC). "Meeting the roadmap will eventually require that process corrections be made on a lot-to-lot, wafer-to-wafer, field-to-field, and site-to-site basis. This will require APC-enabled process tools, with improved access to data and to inputs required for process adjustment."

Applied's Ellwanger says, "APC has enormous potential to improve manufacturing economics. Tighter Cpk and better uniformity are benefits, not to mention longer operating runs within specification. Going further, multitool APC will take wafer data and feed it forward or backward among tools to create sequential process control. This level of APC can potentially tighten process sequence results in ways that even fully optimized single systems cannot."

In a way, APC is the ultimate form of metrology integration. It is expected to apply model-based or proportional process control to reduce process variation, reduce send-ahead and tool monitor wafers, shorten learning cycles and response times, enable better tool matching in high-volume production, improve overall equipment effectiveness, shorten development time, and ease process transfer from pilot line to factory. Future implementations of APC will rely on an industry standard framework of computer-integrated manufacturing to support single-wire integration with the factory manufacturing execution system.

James L. Brissenden, CEO at Inficon, says, "Sensor integration and analysis are at the center of APC technology trends." In situ sensors can provide information about what actually occurs inside process chambers. Residual gas analyzers (RGAs), for example, directly measure process reaction chemistry or process states. RGAs are also capable of measuring wafer states (e.g., outgassing from wafer surfaces). Inficon's experience with its FabGuard in situ analysis solutions has shown substantial process improvements and cost advantages to chip makers.

"A key to effective process control is accurate, repeatable, relevant, and timely measurements," says Joseph Pellegrini, CTO at New Vision Systems (NVS), Cambridge, MA. NVS is engaged with engineering and technology groups at many in situ monitoring and metrology suppliers to optimize process state observation while validating the logistical issues of communication between APC and measurement systems. Pellegrini contends that sensors and metrology tools must provide confident information in addition to raw data for APC to work. "Another major advance is to use multiple sources of data to develop more relevant and accurate process state knowledge. For example, we may see the combination of accurate CD-SEM with sensitive scatterometry metrology to improve CD control," he says.

Wafer cleaning

2001 ITRS challenges surrounding wafer cleaning include providing chemicals with adequate purity levels; interface control, including organic contamination and interfacial oxide; removing ever smaller, difficult-to-reach particles; and post-etch stripping. In addition, other issues overlap wafer cleaning, including chemical and water use reduction and environmental concerns (see "Green rinse and IPA vapor dry," p. 52), yield enhancement, and cycle-time reduction.

Historically, spray processors have had shorter cycle times than immersion benches. To reduce cycle time further, FSI International, Chaska, MN, has developed dilute and ozone chemistry processes that minimize rinse. "Because these chemistries are effective while having a higher water content than conventional chemistries, they are easier to rinse," says Weiping Ma, FSI product marketing manager. "We have reduced the cycle time by more than 30% compared to previous-generation spray processing."

The need to adequately evaluate wafer-cleaning techniques and associated inspection tools, while not directly a cleaning technology, has driven standards activity in particle-size control. Semi standards protocol 3094 mandates that systems used to deposit polystyrene latex spheres (PSLs) for calibrating wafer inspection systems must provide = 3% PSL size and = 5% distribution accuracy.

Engineers at MSP Corp., Minneapolis, MN, have solved complex aerosol problems involved in generating, depositing, sampling, and measuring 3nm to 100&mum particles on wafers. An MSP system uses a differential mobility analyzer to provide NIST sizing via control of electrode voltage and airflow. "We can deposit these test particles as real process particles found as contamination in fabs, such as SiO_2, Al_2O_3, TiO_2, Si_3N_4, Si, Ti, W, and Cu for wet-clean engineers," says MSP's marketing manager John Turner. "This technology also addresses different elevations and temperatures of fabs throughout the world, which can cause small size variations when depositing PSL spheres." The new approach creates a "spot deposition wafer" with known particle types, sizes, and counts at specific locations.

Comparing test results with conventional "dipped wafers," MSP engineers have found that before-and-after wafer inspection scans of dipped wafers do not easily offer the capability to detect or sort out adders and migrating particles caused by the cleaning cycle. However, adders and migrating particles can be easily observed with spot-deposited wafers.

According to Turner, MSP has already determined the influence of wet-clean benches on particles <100nm using the spot-deposition method. This basic knowledge has been used to improve cleaning processes across a broad array of methods at FSI International, Samsung, and others.

Particle Measuring Systems, Boulder, CO, has demonstrated another monitoring technology related to wafer cleaning — a particle monitor capable of a 20% improvement in signal-to-noise ratio when measuring particles in ultrapure water (UPW) at a five-times increase in sample volume. The technology incorporates a unique background count reduction algorithm. The result is 0.035&mum particle sensitivity at a sample volume of 1.2ml/min.

Trace metal impurities

Near-term ITRS requirements call for reducing critical metals in UPW from 20ppt to 10ppt, and in liquid chemicals from 10ppt to 5ppt. Pall Corp., East Hills, NY, has a strong cationic exchange purifier — IonKleen — designed to address this requirement. This purifier technology uses a high-density polyethylene membrane with cationic exchange groups covalently bonded to the membrane surface. By employing a high-surface-area pleated design, the technology is able to provide rapid ion removal without the diffusion delay associated with ion exchange beds.

Table 2. Representative metal ion removal from IPA

Element	Influent (ppb)	After 10 liters (ppb)
Al	0.27	<0.01
Ba	0.11	<0.01
Ca	0.81	<0.01
Cr	0.07	0.05
Cu	0.12	<0.01
Fe	0.17	<0.01
K	0.62	<0.01
Mg	0.04	<0.01
Na	1.51	0.02
Ni	0.22	<0.01
Pb	0.03	<0.01
Zn	0.20	<0.01

Source: Pall Microelectronics

Michael Mesawich, VP of marketing at Pall Microelectronics, says, "The technology can be applied, for example, to DI water, photoresist, and isopropyl alcohol (IPA) with demonstrated metal reduction down to single-digit ppt levels (Table 2), without concerns about ion exchange bead breakdown and loss of precious chemicals within the holdup volume of the exchange column." It is also applicable to polar solvents, such as ethyl lactate, PGMEA, and MIBK, widely used in lithography.

Particles from trenches

More difficult particle removal steps include post-process residues from high-aspect-ratio structures. Brian Fraser, manager of customer applications at Verteq, Santa Ana, CA, notes, "What is needed is a direct 'line of sight' of energy sources to particles in recessed areas, and greater precision in applying energy within the narrowing band between effecting particle removal and causing damage."

Verteq's engineers have modeled and evaluated advance megasonics coupled with single-wafer processing, which achieves significantly improved process uniformity. This is enabling greater selectivity between effecting particle removal and causing damage, and is also enabling rapid process times.

Likewise, advanced developments in Marangoni-based drying optimized for single-wafer processing is enhancing overall process cleanliness by displacing rather than evaporating rinse water, even from high-aspect-ratio structures.

Supercritical stripping, cleaning

Overall, wet chemical cleaning is still favored because many inherent properties of liquid solutions facilitate the removal of metals (high solubility in liquid chemistries) and particles (zeta potential control, shear stress, and efficient energy transfer by megasonics).

However, removing photoresist and residue with supercritical fluids (i.e., CO_2) is one of the 2001 ITRS emerging alternative technologies to the current techniques involving plasma ashing and wet cleaning. David Mount, VP of strategic development at SC Fluids, Nashua, NH, says, "CO_2 has a low critical point — 1070psi at 31°C. In the supercritical state, it is a very powerful solvent, nonflammable, nontoxic, noncorrosive, environmentally benign, and uses no DI water. Most important, it has virtually zero surface tension, so it has the ability to wet and clean the smallest of features identified on the

ITRS. The CO_2 process is functional and very effective in a benign temperature regime (<150°C).

SC Fluids has been working with IBM and International Sematech to demonstrate the viability of supercritical CO_2 ($SCCO_2$) for photoresist residue removal on a variety of thin films, including low-*k* films, where, so far, it is completely compatible. "Considerable effort has also been put into the development of single-wafer process apparatus used to conduct these process developments," says Mount.

Chemistry control

Stringent control of plating chemistry and the buildup of impurities are ITRS challenges for copper processes. The breakdown of organic additives produces process variability and eventually renders a solution useless. Mykrolis Corp., Allen, TX, has combined advanced oxidation and purification technologies that remove organic and ionic impurities from copper-plating solutions, achieving steady-state process chemistry conditions (Fig. 4).

Click here to enlarge image

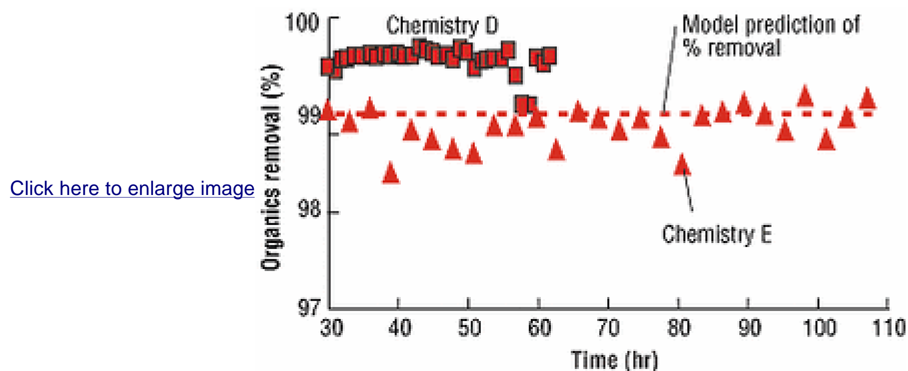


Figure 4. Removal efficiency of plating additives and their breakdown species from copper-plating solutions. (Source: Mykrolis)

"Even in traditional filtration applications, we are facing new challenges," says Jieh Shyu, Mykrolis VP of R&D. Here, the company has new, nonsieving filtration technology — a membrane surface chemically engineered with appropriate zeta potentials and ionic functional groups for a specific application. "A nonsieving membrane design makes it possible to capture extremely small particles and impurities in chemical solutions and solvents, which cannot be done with conventional size-exclusion methods." For example, a nonsieving membrane with average 1000nm pore size can capture 200nm positive and 102nm negative particles.

By modifying the zeta potential of the membrane, it is possible to enhance the capture of extremely small particles of various charges by means of electrostatic and van der Waals forces. "With high mobility of extremely small particles, particle filtration efficiency can achieve near total retention as in gas filtration," says Shyu, "regardless of particle size."

Lithography: Low k_1 and maskmaking infrastructure

Perhaps the biggest problem area going forward on the roadmap is maskmaking. Not only does the industry have to figure out the best ways to deal with the increased mask error factors that come with low k_1 lithography, but, as the roadmap points out, mask linewidth controllability does not meet requirements. The crux of the problem is related to the small mask fabrication market, which limits funding for equipment infrastructure such as mask writers, metrology, inspection tools for substrates and masks, and mask repair tools.

"The infrastructure that makes advanced photomask technology possible doesn't exist," says Paul

Chipman, executive VP of development products at DuPont Photomasks. "Where there was only a single product line of chrome-on-glass photomasks in the past, today's microimaging solutions range from advanced phase shift masks and masks with optical proximity correction, to multiple films, pellicles, and substrates. As a result, there are more variables to control in the maskmaking process and more options that we need to support." Of course, all of this must be resolved at the same time that chipmakers are trying to accelerate development of smaller features.

While there are promising solutions being worked at nodes down to 65nm, what happens after about 2007 — when the industry will be at 65nm and below — is not known. The ITRS specifically calls for solutions for mask process control methods, image placement, and defect density control.

"In 65nm devices, for example, the field poly [which connects the transistor gates to each other] has linewidths at 1/3 the wavelength of light, making it significantly more difficult to produce a clear image on silicon that will result in a working device," explains Buno Pati, CEO of Numerical Technologies. He sees the 90nm and 65nm process generations — with gate lengths of 50nm and 35nm, respectively — as requiring an expansion of phase shifting and a solution to the dilemma of phase conflict, which is the miscoloring of phase shifters so that they form an incorrect silicon image. "These device generations bring the challenges of subwavelength production beyond the transistor gates and into other areas of the chip," states Pati. The company believes that phase shifting is the most commercially viable solution for aggressive feature size reduction on subwavelength ICs.

As companies work on potential solutions to future problems, the industry ekes out all it can from 248nm wavelength lithography, while 193nm lithography struggles with its own infrastructure needs. For example, metrology systems for organic ARC layers that can be used in production volumes, is one such challenge. Xiaohong Chen, product manager at Therma-Wave, reports that closing the gap between research-grade and production metrology tools for 193nm photolithography was tackled in a joint development program with Shipley. Its success is demonstrated by an accuracy comparison using the two types of tools, based on 26 wafers (Fig. 5), which showed no significant differences.

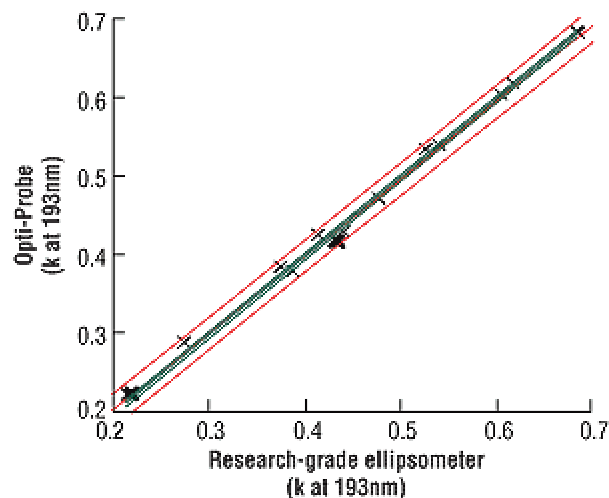


Figure 5. Accuracy comparison of extinction at 193nm for 26 films. (Source: Therma-Wave)

Part of the challenge in staying on the optical lithography roadmap is addressing the changing needs of using the one thing that makes it all possible — light. To stay on the optical roadmap will require continued fine-tuning of laser performance and lens design. Cymer uses its internally developed Lithography Source Requirements roadmap to discern what lies ahead. Using a combination of

measured data on chromatic aberration and simulations, the company models the loss of contrast and consequent variation in CD, which is caused by spectral bandwidth. "The imaging tool parameters for each node are determined from an analysis of projected trends in process requirements for lens numerical aperture and the process factor, k_1," states Nigel Farrar, director of lithography applications at Cymer.

Another industry trend in the quest for better fab productivity is built-in metrology, a key enabler of automatic process control. An example is an optical CD (OCD) tool from Nanometrics for sub-100nm measurements in an Applied Materials etch tool. Excellent correlation with CD-SEMs has been achieved for photoresist trim-CDs using this technology, according to Peter Gise, senior marketing manager for Nanometrics.

Interconnect: Delays and mechanical strength

Lithography is not the only industry segment that is seeing a major shift. The roadmap points out that the Cu/low-*k* transition will minimize the impact of intermediate wiring levels on wiring delay, but the global interconnect dominates RC delay issues. The roadmap consensus indicates that materials changes will not be enough to meet future requirements. The potential for solutions coming from coplanar waveguides, free-space RF, and optical interconnects is noted.

Interconnect delays are seen as a gating item by many. "The transition from aluminum to copper improves device speed by only 30%, while the transition from silicon dioxide dielectric ($k = 4$) to ultra-low-*k* dielectric ($k = 1.5$) improves device speed by as much as 166%," states David Wang, president and CEO at ACM Research. He also points out that technology nodes have accelerated while low-*k* dielectric implementation has decelerated. "If the delay in interconnects is not promptly addressed, device speed will decrease as technology nodes move forward."

As the industry accelerates the move to Cu damascene technology, Cu CMP processes need to be able to address three BEOL material types: Cu/SiO_2, Cu/low-*k* dielectrics, and Cu/ultra-low-*k* dielectrics, according to the roadmap. A major hurdle to overcome, however, is the reduced mechanical strength of porous ultra-low-*k* materials; mechanical forces applied to the wafer during CMP must be reduced. The mechanical strength of copper trench/wire integrated with pure ultra-low-*k* dielectrics decreases by a factor of three every time processes migrate to the next IC-manufacturing node. "The large decrease in mechanical strength of the copper trench structure makes CMP unextendible to the 100nm node and below," says Wang. The company's stress-free copper-polishing process is its answer to the problem facing traditional CMP.

A more basic approach to resolve the mechanical strength issue is to address the fundamental materials challenge. "To a great extent, the cleaning, CMP etch, photoresist poisoning, and adhesion problems encountered in the early stages of low-*k* integration have been solved," states Mark McClear, business director for Dow's Semiconductor Fab Materials Group. "Now, as we look ahead to the 90nm technology node, more advanced problems like optimizing design rules for reliability, production yield, and backend packaging have begun to dominate the low-*k* landscape." Dow Chemical, through its SiLKnet Alliance, is working with both IMEC and ISMT to integrate its new dielectric ($k = 2.0$, with sub-10nm pores) into processes at the 90nm node and beyond.

Click here to enlarge image

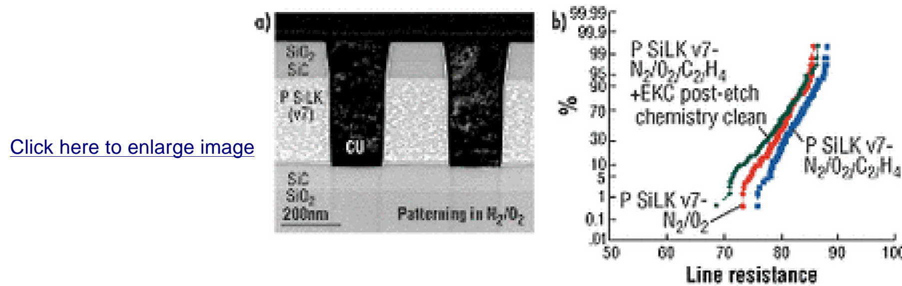


Figure 6. Results of using an EKC cleaning process: a) porous SiLK/Cu structure cleaned with an EKC chemical clean; and b) electrical resistance of a meander for porous SiLK structure, including EKC post-etch chemistry clean. (Source: IMEC)

The growing organic content combined with the increased porosity of low-*k* materials in BEOL ILD poses additional problems. The roadmap highlights the issue of simultaneously minimizing the effective k of the ILD stack and the use of a reduced k etch stop, capping materials, and the need for selectivity. Michael Fury, VP of R&D and engineering at EKC Technology, believes that damascene structures will force changes in etch residue removal and cleaning. "Unfortunately, dry processes, generally used to remove organic materials, are insufficient to remove residues and particles from structures with high aspect ratios without attacking the low-*k* dielectrics or copper barrier," comments Fury. The company has been developing residue removers and other cleaning chemistries that enable the integration of porous low-*k* materials with copper structures (Fig. 6a, b).

Click here to enlarge image

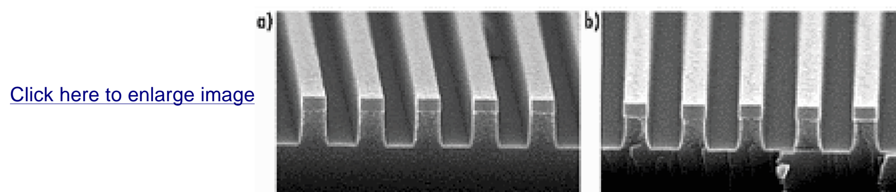


Figure 7. Comparison between optimized and nonoptimized cleaning processes:a) optimized plasma strip and wet clean and drying process of a porous low-k material (MSQ) with a SiC hard mask; and b) nonoptimized process showing a significant low-k attack and k value shift. (Source: Axcelis)

In the case of post-etch cleaning, a conventional clean, drying, and passivation approach can be proven effective over a porous low-*k*/copper stack (Fig. 7), according to data obtained by Axcelis. "Axcelis believes the more conventional cleaning approaches will yield the most manufacturable solutions," states Jan Paul van Maaren, VP and GM of the curing and cleaning systems group.

Use of high-k gate materials, currently under development, will have an impact on the etch process because of their physical and chemical differences from current gate stack materials: SiO and SiN. The roadmap makes specific mention of the difficulty of controlling undercut of profiles, since the high-k gates will be thicker.

Advanced Energy Industries (AEI) sees a critical roadmap challenge in the ability to control the etch profile as CDs get smaller. "For many years, the plasma for this process [plasma etch] was generated by a combination of an RF power supply and a matching network," explains Joe Monkowski, senior VP at AEI. "The matching network was driven by motors, which could take 1-2 seconds to attain the proper setting...and the power was regulated at the output of the power supply, not at the output of the matching network. This allowed variable losses in the matching network to produce variations in the power delivered to the plasma." AEI is supplying subsystems that combine the power supply, a solid-state matching network, and a sensor that measures the power being delivered to the plasma to address

these problems.

Not every interconnect technology challenge is tied to the process itself. A related, yet important one, is how to control costs and performance requirements while introducing new materials, new processes, and new structures. "For CMP liquid management, the roadmap highlights trends toward greater control over planarization performance, reduction in slurry consumption, the need for slurry reuse or recovery, and continued reduction in defects," explains Christopher Case, CTO for BOC Edwards and chair of the Interconnect Working Group for the ITRS. The company has developed point-of-use blenders that enable variable recipe blending for every wafer without prolonged flushing and pumping of polisher and chemical supply systems.

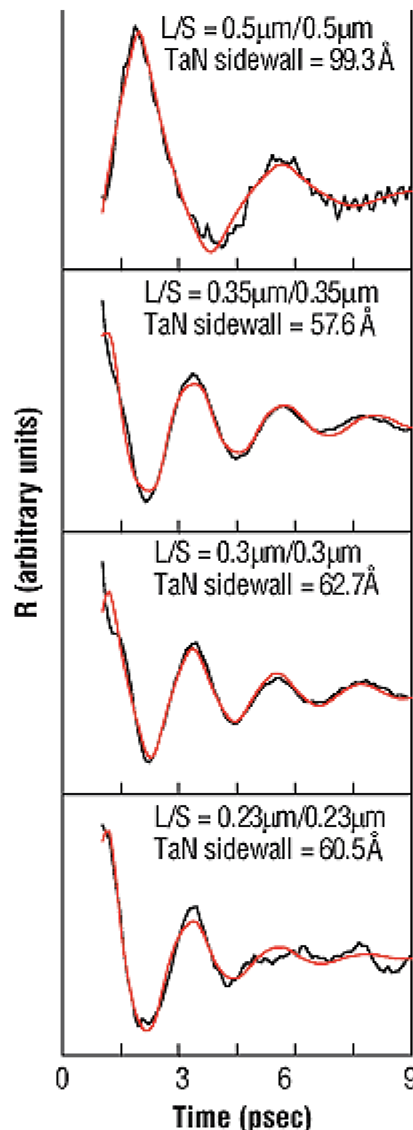
As integration of low-*k* dielectrics proceeds, the chemicals and gas sector has also felt pressure to keep up. Air Products and Chemicals Electronics Division VP and GM Jerry Ermentrout reports that the company is making extensive use of predictive modeling tools to develop precursors that are expected to improve CVD low-*k* film properties, such as film hardness. The company is also working with an SOD technique to create porous films.

low-*k* dielectrics are not the only material challenge for the industry. Regarding the demand for smaller consumer products with longer battery life, EKC Technology's Fury notes that it drives the need for the reduction or elimination of surface-mounted passives, to be replaced by embedded passives on the surface or between the layers of the packaging laminates, and in some cases, in the multilayer interconnect stack on the chip itself. EKC is developing PMOD materials (thin-film high-k [BST] dielectrics for embedded capacitors) for this application, and anticipates the method will be applicable to display technologies. Fury thinks the extreme etch ratios attainable with PMOD may find near-term applications in MEMS and BGA applications, too.

Metrology's link to materials

The combination of 633nm laser ellipsometry and photomultiplier deep-UV reflectometry (DUVR) is proving suitable for measuring 130nm node 15-20Å nitrided gate oxides with <1% repeatability. At the 65nm node, the ITRS needs high-k materials, such as Ta_2O_5 or ZrO_2. Using the same metrology technique, these materials have been measured with excellent repeatability and long-term reproducibility.

The roadmap shows metal electrodes eventually replacing polysilicon. This opaque thin film in the gate stack prevents using ellipsometers for gate process control. Fortunately, acoustic metrology has already shown the ability to simultaneously measure metal gate electrodes and underlying ultra-thin high-k gate dielectrics.



Acoustic vibrations obtained by exciting TaN sidewalls of different linewidths and spacings. The black curve is the measurement signal and the red curve is the fit to measurement.

Ellipsometry with DUVR is also being used to characterize SiGe. To take advantage of SiGe's speed and power requires measuring SiGe film thickness, Ge concentration, Ge depth profile, and, ideally, local stress in the SiGe lattice. Using simultaneous multiple angle of incidence (SMAI) laser ellipsometry, epitaxial SiGe films 2000Å thick having Ge concentrations from 0- 40% are being reliably measured. The process of measuring graded Ge profiles with SMAI will be available in the next few months. Eventually, this capability will be extended to measure stress in the SiGe lattice and dopant concentration by combining ellipsometry with acoustic metrology.

Acoustic metrology can also differentiate between the metallization layer of interest and the underlying structure, allowing accurate measurements on all interconnect levels. The 5x7&mum spot size enables measurements in active regions and in scribe line test sites, with an edge exclusion = 0.5mm. The

current spot size allows measurements on devices having linewidths predicted by the ITRS through the 65nm node. New applications being developed include copper void detection, evaluating via and contact quality, and measuring post-CMP global planarity.

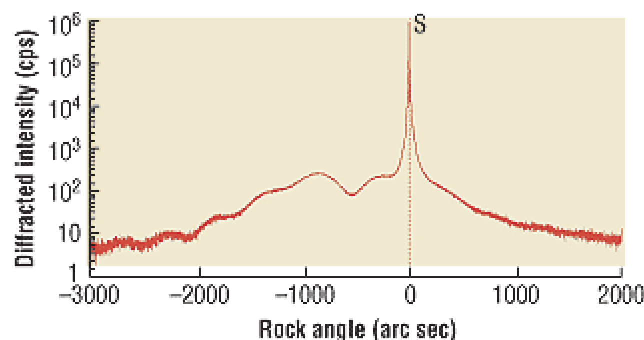
When combined with ellipsometry, acoustic results may be able to provide elastic modulus measurements of low-*k* dielectric materials. This information could help predict the effect of CMP on low-*k* interlayer dielectrics and speed their integration into semiconductor manufacturing.

Acoustic techniques for measuring high-aspect-ratio submicron, 50% dense line arrays predicted by the ITRS are also being refined. This technology can measure copper and dielectric thinning due to erosion as required by the ITRS to the 90nm node and beyond. Barrier materials as thin as 40Å can routinely be measured and work continues for much thinner barriers. Indeed, acoustic technology may enable the critical measurement of barrier sidewall thickness under copper (see figure). Frequency domain analysis may also provide the ability to make CD measurements of copper dual damascene structures.

Guray Tas, Manager, Advanced Systems Development
Rudolph Technologies

ITRS wants to see a small world
Near-atomic-dimension ITRS requirements include ultra-thin gate oxides (UTGOs). Channel lengths below 180nm have gate dielectric thicknesses = 20Å and measurements need subatomic repeatability (e.g., 0.025Å for UTGOs). Engineers at Philips Analytical, Almelo, The Netherlands, have tuned laser ellipsometry combined with reflectometry (LE/R) to measure UTGOs with thicknesses of 16Å and below. This technology extracts optical characteristics and hence, film thickness, very accurately, with a single measurement that has 1s precision of ~0.02Å with a repeatability of 0.025Å. This puts LE/R well ahead of ITRS requirements.

Alec Reader, semiconductor metrology line business manager at Philips Analytical, says, "We have also demonstrated the ability to use x-ray analysis to characterize ultra-thin-film materials like SiGe. The major problem here has been the huge amount of data generated that limited x-ray diffraction to R&D. Processor and software advances, however, now allow fast extraction of layer thickness, Ge content, and grading profile by nonexperts in a production environment."



An x-ray diffraction analysis of an HBT structure with a graded SiGe layer and silicon cap. With the silicon lattice parameter known, the silicon peak is a reference. Differences in lattice parameters come from measuring differences from substrate peaks. Peak separation shows Ge layer concentration; peak

shape shows layer thickness. (Source: Philips Analytical)

SiGe heterojunction bipolar transistor (HBT) emitter sizes are typically sub-0.35&mum for 1-5 GHz applications. The figure shows a full SiGe HBT structure with an SiGe graded layer and silicon cap. The peak is asymmetric, and the intensity modulations are caused by absolute thickness of the layers. From these curves, software provides an unambiguous measurement of layer composition and thickness.

Alec Reader
Philips Analytical

Cutting-edge analytical laboratory capability
New methods can provide detection limits (DLs) below the roadmap values of 10^9atoms/cm^2 for critical metals on 300mm wafers. These methods include using vapor phase decomposition, inductively coupled mass spectroscopy (VPD ICP-MS; see "Enhanced ICP-MS for trace metal purity levels," p. 56); VPD total reflection x-ray fluorescence (VPD-TXRF); and synchrotron TXRF technologies in research and production.

The 2001 ITRS indicates organic limits at wafer interfaces at ~$2.1x10^{13}$ carbon atoms/cm$_2$ for 2002. For the semivolatile organics that adsorb onto wafers and that originate from air, gases, and process tools, full wafer analysis on silicon witness-wafer surfaces using ASTM methodology can meet the roadmap requirement levels out to 2007. Problems — such as delamination of photoresist, metals, and other layers; gate oxide metrology errors; and doping difficulties — due to organic contamination have been solved using this method, which can quantitate organics and identify individual compounds even in mixtures.

Copper processes analysis
The collection solution used in wafer analysis by VPD is critical for efficient copper (Cu) characterization. Newly implemented special solutions and procedures provide lower DLs by ensuring better Cu recovery. Analysis of trace metal contamination in copper films (difficult because of the high copper concentration) can also be performed on a routine basis by dissolution of the copper film followed by ICP-MS.

In addition to wafer and thin-film analyses, Cu processes require analytical testing to control incoming solutions and plating baths. New analytical methods provide routine quantitative analysis of corrosion inhibitors both off-line and in-line at fabs. Cu contamination can be devastating at process critical points in the fab, which necessitate witness-wafer and wipe analyses.

Plating chemistries
Although used for years in lower technology-plating applications, electroplating processes used in new fab procedures require stringent analytical control. Cyclic voltammetric stripping (CVS) for organic additive analysis, mentioned in the ITRS, has been used in a production mode for five different Cu and PbSn plating chemistries. Analysis of additional parameters (i.e., Cu, Pb, Sn, Au, Pd, and Ni) and other inorganic and organic components in various plating chemistries has also been implemented as a production procedure. All of these analyses are used to characterize electroplating processes better. Considerable interest is now focused on developing liquid chromatography methods for determining specific breakdown products that affect plating efficiency.

low-*k* materials
The roadmap states "little understanding exists regarding impurity specifications." New methods,

however, have answered customer requests and quantified starting reactant chemicals as well as by-product contaminants that go into the production and purification of low-*k* materials.

Ultrapure water
The ITRS specifies maximum near-term levels of 20ppt for critical cations, anions, and metals. Current DLs meet all near-term levels of 20ppt for contamination control. Using new methods and instruments, we can now also detect the 10ppt level, projected out to 2007, for all metals.

Finally, our recent work on measuring native oxide levels at or below a monolayer level has shown that concentrations of dissolved oxygen in ultrapure water can create unsuitable conditions for polysilicon deposition.

Scott Anderson, Director of R&D, Balazs Analytical Services, Air Liquide

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Unified AMHS
Heading into 2004, "manufacturable solutions" are not known for many 2001 ITRS processes. These include elements of factory ramps, equipment lead time, factory cycle time, throughput, maintenance, material handling, and the interconnected importance of factory information and control hardware and software.

Specifically, for material handling, the ITRS requires that automated material-handling systems (AMHS) must interface directly with all 300mm tools used in a normal production process flow, while providing acceptable return on investment. "

Solutions to provide higher wafer storage densities, short lead and install times, and better utilization of floor space through integration of process and metrology equipment must be developed."

The ITRS specifically states the need to combine interbay and intrabay AMHS into one integrated capability (i.e., a "unified" tool-to-tool transport system that replaces conventional "segregated" interbay and intrabay approaches). This must be all done within the context of lower failure rates and faster repairs; substantially increased throughput; and designs that accommodate extendibility, flexibility, and scalability demands on the factory.

Using discrete event simulation, engineers at PRI Automation have evaluated 300mm fabs with fully unified AMHS (a single overhead transport [OHT] system throughout the fab), partially unified (still using interbay transport, but with several bays of OHT "linked" together), and a combination of both, all compared to segregated AMHS.

Their data for a bay-chase fab (see table), for example, clearly showed that total material-handling moves were fewer for the unified configuration simply because every tool-to-tool unified move

requires only two transports, as opposed to three in a segregated configuration. Although the total required storage space for work in progress (WIP) is the same for each configuration (WIP level is driven by manufacturing factors, not AMHS design), the number of stocker cycles required to accomplish lot moves decreases for a fully unified system. In the modeled segregated system, 22 stockers were required because at least one stocker was needed in each bay (bays with high intrabay activity and lot move frequency require more stockers). But the unified system required only 15 stockers, since less stocker work is required and adjacent bays can share stockers.

Simulated comparison of segregated vs. unified AMHS*

Fab data	Segregated	Unified
Lot moves/hr (= process steps/hr)	762	762
Interbay	511	0
Intrabay	251	762
AMHS work required		
Stocker cycles/hr	2035	1524
OHV moves/hr	1524	1524
OHS moves/hr	511	0
AMHS equipment		
Stocker quantity	22	15
Avg. stocker utilization	41.1%	49.4%
OHS vehicle quantity	x	0
OHT vehicle quantity	1.7x	2.4x
Total vehicles	2.7x	2.4x
Relative system eMTBF	y	1.11y
Relative cost	z	0.87z

*for a bay-chase fab capable of 43,000 wafer starts/month, 762 process steps/hr, and equipped with 17 bays and storage for 3700 lots

As a result of lower stocker requirements, system costs for linked and unified configurations are less. More overhead vehicles (OHVs) are required in the unified than any other configuration. However, fewer overall vehicles are needed with a unified system. This number could further decrease as more intelligence is added to vehicle dispatch systems and as real-time scheduled data are integrated with the material control system.

PRI engineers concluded from this work that unified AMHS had the highest mean time between failures (MTBF) and lowest system cost. The former correlated with fewer system components and the latter directly related to the need for fewer stockers. Conventional segregated AMHS requires more stockers to support individual intrabay loops and handle more total lot moves. A unified approach also enabled more flexible tool placement with a saving of fab floor space; for example, a unified configuration takes advantage of the chase for repositioning metrology tools so they can be shared between two bays. In addition, unified AMHS provided shorter tool-to-tool average delivery times — 32% lower for normal lots, 66% lower for hot lots. Lower delivery times for unified AMHS are due to fewer lot hand-offs; this shortens the total transport and handling times and eliminates queue times for these unneeded hand-offs.

According to Joe Reiss, director of strategic marketing for PRI Automation, Billerica, MA, it is generally accepted that the primary challenge to implementing unified AMHS is the sophisticated

control software required. However, Reiss notes that PRI's simulations were run using the same control algorithms found in PRI's existing AMHS transport control and MCS software. "In addition to showing the performance benefits of unified AMHS, our simulations demonstrate the ability of the AMHS software to manage the complex move-routing task of a single, large-scale transport network," he says.

These engineers are investigating the effect of AMHS configurations on fab performance using full-fab simulation. One fab configuration under evaluation is that used in an International Sematech study that looked at various tool layouts considered for a 300mm fab. They are currently examining effects of unified AMHS on wafer cycle time and equipment utilization.

Pieter "Pete" Burggraaf, Senior Technical Editor

Courtesy: PRI Automation

Green rinse and IPA vapor dry
GreenDry from SCP Global combines isopropyl alcohol (IPA) vapor generation, a rinse tank inside a dryer enclosure, and a drain and exhaust subsystem. Wafers go directly into a rinse cycle starting with the tank filled with DI water. The tank is dumped and drying is via IPA vapor condensation that replaces surface water. A 50-wafer-lot process was done in 9 min using ~100 liters of rinse water and <100ml of IPA. This run achieved (with 1mm edge exclusion):

- particle neutrality for hydrophilic surfaces down to 0.09&mum, and
- particle adders for hydrophobic surfaces <20 at >0.09&mum.

Further, both optical and AFM inspection confirmed no water marks after using this drying technology on 40:1 aspect-ratio deep trenches (i.e., hydrophobic etched trenches in silicon and a hydrophilic SiO_2-Si_3N_4 top layer).

Jagdish Prasad, worldwide product applications manager at SCP Global Technologies, Boise, ID, notes that the GreenDry process can also inject dilute HCl to adjust pH during rinse, achieving ITRS metal requirements of $5x10^9$ atoms/cm_2.

Enhanced ICP-MS for trace metal purity levels
Inductively coupled plasma mass spectrometry (ICP-MS) has a reputation as the most sensitive trace element technique. It is being used routinely to analyze high-purity process chemicals, gases, and also to measure metallic impurities on silicon wafers.

However, for many of the metals important to the semiconductor industry, spectral interferences severely limit ICP-MS to ultralow detection limits. For example, the lowest detection capability achievable for iron is at the most abundant isotope (^{56}Fe). Unfortunately, in the process of generating ^{56}Fe ions, the argon plasma and the sample also produce large numbers of mass 56 argon oxide ions. Low ppt detection limits for ^{56}Fe can only be obtained if the $^{40}Ar^{16}O$ ions are removed.

Although different techniques have been used to remove such interferences, they have not lowered background levels enough to achieve single-figure ppt detection limits demanded for next-generation ITRS purity levels. There is a new approach — dynamic reaction cell (DRC) technology — that addresses many of these problems.

The device, consisting of a quadrupole contained within a reaction cell, is placed between the ion-

focusing system and the mass analyzer. A reactive gas is bled into the cell to cleanse the ion beam of interferences, while allowing analyte ions to proceed to the mass analyzer for measurement. This "chemical resolution" process clears the way for the majority of semiconductor elements to be measured at low ppt levels, regardless of the material being analyzed.

DRC metal detection limits		
Element (ppt)	DL (ppt)	BEC
Li	0.26	0.22
As	0.48	1.6
B	1.93	1.50
Na	0.14	0.22
Mg	0.08	0.18
Al	0.05	0.09
K	0.27	2.60
Ca	0.10	0.10
Ti	0.92	1.70
V	0.12	0.04
Cr	0.12	0.12
Mn	0.17	0.54
Fe	0.12	0.40
Ni	0.10	0.20
Co	0.04	0.04
Cu	0.05	0.10
Zn	0.45	1.20
Sn	0.12	0.88
Sb	0.08	0.08
Ba	0.06	0.04
Pb	0.07	0.09

With DRC technology, analytical methods have been developed on the ELAN DRC II for important process chemicals and materials, including hydrogen peroxide, sulfuric acid, phosphoric acid, and IPA, and for metallic contamination on silicon wafers (see table).

David Armstrong, Semiconductor Business Manager, PerkinElmer Instruments

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Ion implant gets tougher
A roadmap discussion would not be complete without a look at the usually slow-changing ion implant sector. This segment is gearing up for a projected CAGR of some 24% — up to US$2.433 billion by 2006.

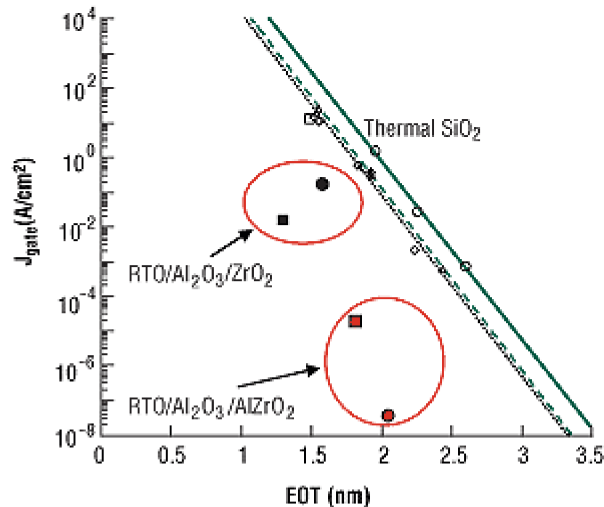
Each of the "big three" equipment makers — Applied Materials, Axcelis, and Varian Semiconductor Equipment Associates (VSEA) — have plans on how to address the main challenges facing this market within the context of a total fab management strategy: doping accuracy, flexibility (single-wafer vs. batch, or multiwafer tools), and productivity.

The roadmap highlights the need for greater attention to precision doping as well as thermal budget constraints — pre- and post-process. "As devices scale, thermal budget constraints in the process flow will reduce the level of dopant activation in the device," notes Ernest Godshalk, president and COO of VSEA. "As a result, to increase the dopant level in silicon, higher dose implants with higher activation techniques are needed. This constraint, coupled with the need for high-productivity implantation at ultra-low ion energies, can best be solved by plasma doping."

IMEC tackles scaling

The CMOS scaling challenge is being addressed by IMEC in two ways. The first path is finding a high-k replacement for SiO_2. The second is finding a more economical way to manufacture ICs.

"Many people think that the most significant challenge for device scaling and perpetuation of Moore's Law will not be a technical barrier, but a cost reduction for manufacturing ICs," notes Ludo Deferm, VP of business development at IMEC. "To allow a reduction in cost/function, which is the fuel behind the semiconductor industry, it is important to note that the rate of increase of components/chip is greater than the rate of increase of cost/chip."



Binary and mixed oxides with poly gate. ALCVD-deposited layers with in situ poly-Si. Note the reduced leakage currents for equivalent EOT stacks compared to SiO_2.

Deferm believes that the key to cost reduction for new process cycles is to focus on integration. "CMOS will always stay the basic technology, but new integration technologies, like SiP and SoC, can be used to allow cost reduction." Innovations in packaging and design technology will also be necessary to make cost reductions a reality.

IMEC's search for a high-k gate dielectric material has focused on Al_2O_3, HfO_2, ZrO_2 and other mixtures, such as aluminates and silicate alloys. "The use of mixed oxides of the higher-k HfO_2 or ZrO_2 and the stable Al_2O_3 resulted in enhanced resistance to crystallization, low EOT (equivalent oxide thickness) values, and low leakage currents," reports Marc Heyns, director of IMEC's department of ultraclean processing, high-k dielectrics, EPI, and ES&H (see figure). "For low-standby power applications, where EOT values in the range from 1.2nm up to 1.6nm are targeted, these results are very promising."

More work needs to be done to optimize results toward low EOT values. Specifically, additional studies remain to improve the properties of the interface between the silicon and the high-k layer.

Design debug

The tremendous pressure on IC manufacturers to accelerate time-to-market requires a more integrated approach to the entire IC design, manufacture, and test cycle. To that end, design debug is undergoing changes along with the rest of the process side of the business, brought about by the transitions to new materials. "

In the near term, internal debug editing must deal with copper and low-*k* dielectrics," explains M. Leibowitz, director of probe systems' advanced technologies at Schlumberger Semiconductor Solutions. "While copper with SiO_2 and FSG is no longer a challenge, organic low-*k* materials respond differently and have not been fully addressed. Organic low-*k* can quickly degrade under charged particle imaging."

On the bright side, Leibowitz notes that high-k gate dielectrics do not need to be addressed because they are never the subject of edits. Additionally, the new, complex interconnect concepts that allow access to the silicon side do not affect present debug strategies. Future challenges include possible optical and nanotube interconnects.

Fab planning
Along with the industry transitions to new materials, 300mm wafers, and the attendant need for automated process lines, is the added burden of increased sensitivity of reticles to handling and ESD-related damage.

Clint Haris, director of lithography automation at Brooks Automation, says that the combination of these factors and leading-edge IC manufacturers' growing need to stock greater numbers of reticles, can be addressed with automated reticle sorting, stocking, and delivery systems in fabs. Fabs are also starting to implement automated methodologies to maximize the use of existing tool sets.

A different view of the roadmap
The conventional view of the industry roadmap is to see it as a combination of leaps and bounds that ultimately ends with feature shrinks, utilization targets, or the introduction of new materials.

Another way to view the progress, however, is by market segment, i.e., consumer electronics, PCs, wireless communications, etc. When Applied Materials undertook this exercise, it discovered the kinds of products that best address the fastest growing segment in the fab market — the fab foundry — and, in particular, the high-end foundries that overlap with advanced microprocessor and DSP fabs.

Accordingly, the company is staking its business strategy on three product types: pre-integrated process modules to address copper interconnects; defect detection and defect review SEMs with FIB-sectioning capability; and single-wafer CVD ALD and thermal oxidation for transistor structures.

For DRAM applications, advanced sub-100nm devices will have two areas of convergence with advanced logic, notes Ashok Sinha, senior VP of Applied's silicon business sector products. "First, certain chipmakers will gain performance advantages by embedding DRAM into logic for SoCs," explains Sinha. "Second, the metallization scheme will shift from a possible three-layer metal Al-based to a two-layer metal Cu-based."

Ashok Sinha
Applied Materials

Solid State Technology May, 2002
Author(s) : SST Staff

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There are many paths to yield.